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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	21

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/536,452	Applicant(s) RONEN ET AL.
	Examiner David J. Huisman	Art Unit 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-15 and 17-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-15 and 17-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 4-15, and 17-23 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: #19 RCE as received on 5/6/2004 and #20. Pre-Amendment "F" as received on 5/6/2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 4-15, and 17-23 is rejected under 35 U.S.C. 102(b) as being anticipated by Killian et al., U.S. Patent No. 5,420,992 (as applied in the previous Office Action and herein referred to as Killian).

5. Referring to claim 1, Killian has taught a processor comprising:

a) means for executing an instruction of an application of a first bit size ported to a second bit size environment, the second bit size being greater than the first bit size. See column 2, lines 7-33.

b) means for confining the application to a first bit size address space subset (see column 19, lines 36-40), said means for confining comprising:

(i) means for truncating generated address references of the second bit size to the first bit size. See Fig.5D and note that the 64-bit virtual address is truncated by removing the upper 32 bits of the address (VA(63..32)), which are then sent to a multiplexer 172.

(ii) means for extending to the second bit size the truncated generated address references based at least in part on a setting of an address format control signal, a first setting of the address format control signal to indicate zero-extension of the truncated generated address references and a second setting of the address format control signal to indicate sign-extension of the truncated generated address references. Looking at Fig.5D, it should be realized that the virtual address is in sign-extended form (column 17, lines 15-24). The upper 32 bits of the address (sign extension bits) are then separated from the rest of the address and fed into the multiplexer 172, thereby truncating the virtual address. As seen from Fig.5D, the multiplexer would then have two 32-bit inputs; the first being 32 zeroes and the second being the 32 sign-extension bits. One of the inputs will be selected by the multiplexer, resulting in either zero-extending (if the 32 zeroes are selected) or sign-extending (if the 32 sign bits are selected) the truncated virtual address. A single signal, i.e., the "32-bit user mode" signal, is used to determine the output of the multiplexer. That is, this signal (i.e., address format control signal) will select either zero-extension or sign-extension of the address.

6. Referring to claim 2, Killian has taught a processor as described in claim 1. Killian has further taught that the first bit size is 32-bit and the second bit size is 64-bit. See column 3, lines 30-31, and column 5, lines 8-19.

7. Referring to claim 4, Killian has taught a processor as described in claim 1. Killian has further taught that the means for confining includes means for generating an address fault. See column 11, lines 3-5. The 32-bit address (which would be represented as an extended 64-bit number in the 64-bit environment) that is used to select a memory location in the address space subset is checked for a certain value and if that value exists, then an address error exception will occur.

8. Referring to claim 5, Killian has taught a processor as described in claim 1. Killian has further taught that the means for extending includes means for determining that the first bit size address space subset is signed address space. See column 19, lines 36-40. From this passage it can be seen that the address space is from -2^{31} to $(2^{31}-1)$ which is also known as –2GB to +2GB.

9. Referring to claim 6, Killian has taught a processor as described in claim 1. Killian has further taught that the means for extending includes means for determining that the first bit size address space subset is unsigned address space. See column 13, lines 10-27, and Table 3A. Killian has disclosed Load-Byte-Unsigned (LBU) and Load-Halfword-Unsigned (LHU) instructions, which are zero-extended as opposed to sign extended. As an example, LBU will retrieve an 8-bit value from memory/cache, and zero-extend it to 64-bits, regardless of the most significant bit position. If this unsigned data were then used as an address to access memory, which is possible since Killian has also disclosed indirect jumps in Table 5B (where the contents of a specified register are used as an address to access memory), it would follow that the address space would be unsigned.

10. Referring to claim 7, Killian has taught a processor comprising:

a) a memory to store an instruction of an application ported from a first bit size environment to a second bit size environment, the second bit size being greater than the first bit size. See Fig.1 and column 7, lines 49-54. Note the existence of main memory and an instruction cache.

b) an instruction execution core coupled to said memory, said instruction execution core to execute the instruction of the application. See Fig.1. Note that data and instructions are retrieved from memory/cache by the EIC (component 25) and propagated along bus 30 to the execution unit.

c) said instruction execution core to determine that the application is confined to a first bit size address space subset. See column 19, lines 36-40.

d) said instruction execution core to generate an address reference of the second bit size as part of execution of the instruction. See column 12, lines 26-65. Also, see Fig.5D and note that a virtual address is generated (at the middle of the page).

e) said instruction execution core to truncate the generated address reference from the second bit size to the first bit size. See Fig.5D and note that the 64-bit virtual address is truncated by removing the upper 32 bits of the address (VA(63..32)), which are then sent to a multiplexer 172.

f) said instruction execution core to extend the truncated, generated address reference from the first bit size to the second bit size based at least in part on a setting of an address format control signal, a first setting of the address format control signal to indicate zero-extension of the truncated generated address reference and a second setting of the address format control signal to indicate sign-extension of the truncated generated address reference. Looking at Fig.5D, it should be realized that the virtual address is in sign-extended form (column 17, lines 15-24). The upper 32 bits of the address (sign extension bits) are then separated from the rest of the

address and fed into the multiplexer 172, thereby truncating the virtual address. As seen from Fig.5D, the multiplexer would then have two 32-bit inputs; the first being 32 zeroes and the second being the 32 sign-extension bits. One of the inputs will be selected by the multiplexer, resulting in either zero-extending (if the 32 zeroes are selected) or sign-extending (if the 32 sign bits are selected) the truncated virtual address. A single signal, i.e., the "32-bit user mode" signal, is used to determine the output of the multiplexer. That is, this signal (i.e., address format control signal) will select either zero-extension or sign-extension of the address.

11. Referring to claim 8, Killian has taught a processor as described in claim 7. Killian has further taught that the application ported from a first bit size environment to a second bit size environment is an application ported from a 32-bit environment to a 64-bit environment. See column 3, lines 30-31, and column 5, lines 8-19.

12. Referring to claim 9, Killian has taught a processor as described in claim 7. Killian has further taught that the instruction execution core is to determine that the application is confined to a first bit size address space subset based at least in part on an address space control flag. See column 17, lines 25-27. Note from columns 17-19, that based on the different modes, different address space subsets are used.

13. Referring to claim 10, Killian has taught a processor as described in claim 7. Killian has further taught that the instruction execution core is to extend the truncated, generated address reference from the first bit size to the second bit size based at least in part on an address format control flag. Recall from the very top of Fig.5E of Killian that a "32-bit user mode" signal exists. This signal, when set, would indicate that addresses should be zero-extended and when cleared would indicate that addresses should be sign-extended. Furthermore, this signal will be

stored as a flag in a status register, which is described in column 17, lines 25-31. This register comprises flags which specify parameters of the system including the bit-mode (32 or 64) in which the system operates and the type of mode (user, supervisor, kernel) in which it operates. Therefore, the "32-bit user mode" flag will originate in the status register.

14. Referring to claim 11, Killian has taught a processor as described in claim 7. Killian has further taught that the instruction execution core is to generate an address fault flag based at least in part on a comparison of the generated address reference and the extended, truncated, generated address reference. Recall from previous rejections that a generated 32-bit number is extended to a 64-bit number in Killian's system. From column 17, line 61, to column 18, line 7, Killian has disclosed that bit 31 of the 64-bit number is checked. If that value is 0, then an address fault has not occurred. However, if that value is 1, then an address exception has occurred. Bit 31, in a sense, represents an overflow bit in that when that bit is set, then the 32-bit application has crossed the 32-bit address space boundary and a fault has occurred. It should be noted that a comparison would inherently be performed to check bit 31. And, this comparison is related to both the original 32-bit address and the extended 64-bit version.

15. Referring to claim 12, Killian has taught a processor as described in claim 11. Killian has further taught that the instruction execution core is to generate an address fault flag based at least in part on an address fault control flag. See Fig.5E. In the upper-right corner of the figure, different types of address faults (R3ERR, R2ERR, R1ERR, and R0ERR) are coupled to a multiplexer which is controlled by an address fault control flag VA(63..62). This value is used to help generate an address fault flag (output line denoted as ADDRESS ERROR), if one exists for the corresponding mode.

16. Referring to claim 13, Killian has taught a processor as described in claim 7. Killian has further taught that the memory is a cache memory. See column 7, lines 50-52.

17. Referring to claim 14, Killian has taught a processor as described in claim 7. Killian has further taught that the processor is a 64-bit processor. See column 2, lines 16-41, and column 3, lines 30-31. Killian has disclosed that the registers and data path, along with memory addresses, are 64 bits wide. Therefore, Killian has taught a 64-bit processor.

18. Referring to claim 15, Killian has taught a method to confine an application to an address space subset, the method comprising the steps performed by the processor of claim 7. Therefore, claim 15 is rejected for the same reasons set forth in the rejection of claim 7.

19. Referring to claim 17, Killian has taught a method as described in claim 16. Furthermore, claim 17 is rejected for the same reasons set forth in the rejection of claim 8.

20. Referring to claim 18, Killian has taught a method as described in claim 15. Furthermore, claim 18 is rejected for the same reasons set forth in the rejection of claim 9.

21. Referring to claim 19, Killian has taught a method as described in claim 15. Furthermore, claim 19 is rejected for the same reasons set forth in the rejection of claim 10.

22. Referring to claim 20, Killian has taught a method as described in claim 15. Killian has further taught that extending the truncated, generated address reference from the first bit size to the second bit size includes sign-extending the truncated, generated address reference from the first bit size to the second bit size based at least in part on the address format control flag. Recall from the very top of Fig.5E of Killian that a "32-bit user mode" signal exists. This signal, when set, would indicate that addresses should be zero-extended and when cleared would indicate that addresses should be sign-extended. See column 3, line 67, to column 4, line 10. Furthermore,

this signal will be stored as a flag in a status register, which is described in column 17, lines 25-31. This register comprises flags which specify parameters of the system including the bit-mode (32 or 64) in which the system operates and the type of mode (user, supervisor, kernel) in which it operates. Therefore, the "32-bit user mode" flag will originate in the status register.

23. Referring to claim 21, Killian has taught a method as described in claim 15. Killian has further taught that extending the truncated, generated address reference from the first bit size to the second bit size includes zero-extending the truncated, generated address reference from the first bit size to the second bit size based at least in part on the address format control flag. Recall from the very top of Fig.5E of Killian that a "32-bit user mode" signal exists. This signal, when set, would indicate that addresses should be zero-extended and when cleared would indicate that addresses should be sign-extended. See column 3, line 67, to column 4, line 10. Furthermore, this signal will be stored as a flag in a status register, which is described in column 17, lines 25-31. This register comprises flags which specify parameters of the system including the bit-mode (32 or 64) in which the system operates and the type of mode (user, supervisor, kernel) in which it operates. Therefore, the "32-bit user mode" flag will originate in the status register.

24. Referring to claim 22, Killian has taught a method as described in claim 15. Furthermore, the processor of claim 11 performs the method of claim 22. Therefore, claim 22 is rejected for the same reasons set forth in the rejection of claim 11.

25. Referring to claim 23, Killian has taught a method as described in claim 22. Furthermore, the processor of claim 12 performs the method of claim 23. Therefore, claim 23 is rejected for the same reasons set forth in the rejection of claim 12.

Comments

26. In applicant's interview summary, applicant states that "the examiner agreed not to issue a first office action final rejection in the RCE." The examiner asserts that such an agreement was not made. Instead, the examiner said that a first action final rejection would not be given if the applicant amended the claims such that the scopes of the claims were narrowed in any way. Applicant has failed to do make such amendments, and therefore, a first action final may have been given. However, the examiner has refrained from doing so since modifications, although not major, have been made to the rejections. Furthermore, the examiner has not submitted an interview summary because the applicant spoke of modifying the submitted after-final arguments as opposed to specific claim limitations.

Response to Arguments

27. Applicant's arguments filed on May 6, 2004, have been fully considered but they are not persuasive.

28. In the remarks, Applicant argues the novelty/rejection of claim 1 on pages 7-8 of the remarks, in substance that:

> "Killian does not disclose or suggest "means for extending to the second bit size the truncated generated address references based at least in part on a setting of an address format control signal, a first setting of the address format control signal to indicate zero-extension of the truncated generated address references and a second setting of the address format control signal to indicate sign-extension of the truncated generated address references. Instead, Killian uses separate sign-extension hardware and zeroing circuitry to sign-extend and zero-extend, respectively, the output addresses. In addition, the sign extension hardware and the zeroing circuitry operate independently. In other words, no single signal indicates to the sign-extension hardware to sign-extend on one value and to the zeroing circuitry to zero-extend on another value of the signal."
>
> "...the zeroing circuitry is only operating on the (N-m) most significant bits and not the truncated generated address references."

29. These arguments are not found persuasive for the following reasons:

a) Regarding the first argument, looking at Fig.5D, it should be realized that the virtual address is in sign-extended form (column 17, lines 15-24). The upper 32 bits of the address (sign extension bits) are then separated from the rest of the address and fed into the multiplexer 172, thereby truncating the virtual address. As seen from Fig.5D, the multiplexer would then have two 32-bit inputs; the first being 32 zeroes and the second being the 32 sign-extension bits. One of the inputs will be selected by the multiplexer, resulting in either zero-extending (if the 32 zeroes are selected) or sign-extending (if the 32 sign bits are selected) the truncated virtual address. A single signal, i.e., the "32-bit user mode" signal, is used to determine the output of the multiplexer. That is, this signal (i.e., address format control signal) will select either zero-extension or sign-extension of the address. So, it is clear that a single signal is used to perform either zero or sign extension on a truncated address.

b) Regarding the second argument, the multiplexer 172 of Fig.5D may output 32 zeroes for combination with the truncated address. Therefore, the "zeroing circuitry" does operate on the truncated address by adding (N-m) most significant bits to it.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
June 21, 2004

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